

fractional portion of the wafer, such fractional portion of the wafer having a plurality of electrical contacts;

(ii) an electrical conductor electrically connected to the plurality of electrical contacts of the plurality of chips to electrically interconnect such plurality of chips, portions of the electrical conductor spanning the regions in the fractional portion of the wafer; and

(iii) a plurality of voltage generators, each one being associated with, and disposed adjacent to, a corresponding one of the chips; and

(C) a conductor for electrically connecting the electrical conductor of the package to the electrical interconnect of the printed circuit board.

²¹/₂₇ (NEW) The semiconductor packaging arrangement recited in claim ²⁰/₂₁ wherein each one of the voltage generators is disposed in the separating region.

REMARKS

The above-identified patent application has been amended and reconsideration and re-examination are hereby requested.

It is first noted that claims 8-15 have been amended as dependent claims. The claims are dependent on claims under examination. Therefore, such amended, now dependent claims, are no longer withdrawn from consideration.

Claim 6 stands rejected under 35 U. S. C. 103 (a) as being unpatentable over Tagaya eor Egawa in view of Murari et al. Claim 6 points out that the semiconductor, comprising:

an electrical conductor electrically connecting the plurality of electrical selected one or ones of the electrical components to the chips with portions of the electrical conductor elevated above the regions in the fractional portion of the wafer and spanning the separating regions between the chips in the fractional portion of the wafer.

It is respectfully submitted that the conductor of Muratri et al. does not span the separating regions between the chips in the fractional portion of the wafer as set forth in claim 6.

Claim 1 points out that " portions of the dielectric member with portions of the

electrical conductor thereon spanning the regions in the wafer". Claim 16 points out that "such electrical conductor being electrically connected to the plurality of electrical contacts to electrically interconnect such plurality of chips, portions of the electrical conductor spanning the regions in the fractional portion of the wafer".

Claim 18 points out that "portions of the electrical conductor spanning the regions in the fractional portion of the wafer, such conductor being elevated above the regions in the fractional portion of the wafer". Claim 21 points out that "portions of the electrical conductor spanning the regions in the fractional portion of the wafer".

It is respectfully submitted that the conductor of Muratri et al. does not span the separating regions between the chips in the fractional portion of the wafer as set forth in the claims as noted above.

In the event any additional fee is required, please charge such amount to Patent and Trademark Office Deposit Account No. 50-0845.

Respectfully submitted,

Date

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Richard M. Sharkansky

Attorney for Applicant(s)

Reg. No.: 25,800

Daly, Crowley, & Mofford, LLP

275 Turnpike Street, Suite 101

Canton, MA 02021-2310

Telephone: (781) 401-9988, 23

Facsimile: (781) 401-9966

Attachment: Claim Mark Up Sheets

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COMPARISON CLAIMS

1. (Three Times Amended) A semiconductor, comprising:

a ~~fractional portion of a semiconductor wafer having a plurality of integrated circuit chips thereon, such chips being separated by separating regions in the fractional portion of the wafer, such wafer having a plurality of electrical contacts;~~

a dielectric member having an electrical conductor thereon, such electrical conductor being elevated above the regions in the fractional portion of the wafer, such electrical conductor being electrically connected to the plurality of electrical contacts to electrically interconnect such plurality of chips, portions of the dielectric member with portions of the electrical conductor thereon spanning the regions in the wafer;
and

a plurality of voltage generators, each one being associated with, and disposed adjacent to, a corresponding one of the chips.

3. The semiconductor recited in claim 2 wherein each one of the voltage generators is disposed in the separating region.

~~5. The semiconductor recited in claim 1 wherein each one of the voltage generators has an electrical contact and wherein the semiconductor further includes:
a dielectric member having an electrical conductor thereon, such electrical conductor being elevated above the regions in the fractional portion of the wafer and electrically connected to the plurality of electrical contacts of the plurality of chips to electrically interconnect such plurality of chips, portions of the electrical conductor spanning the regions in the fractional portion of the wafer.~~

6. (Amended) A semiconductor, comprising:

a fractional portion of a semiconductor wafer having a plurality of integrated circuit chips thereon, such chips being separated by separating regions in the fractional portion of the wafer;

a plurality of sets of electrical components, each set being associated with, and adjacent to, a corresponding one of the chips; and

an electrical conductor electrically connecting the plurality of electrical selected one or ones of the electrical components to the chips with portions of the electrical conductor elevated above the regions in the fractional portion of the wafer and spanning the separating regions between the chips in the fractional portion of the wafer.

7. The semiconductor recited in claim 6 wherein each set of electrical components includes a plurality of different electrical components.

10. (Amended) TheA semiconductor recited in claim 6 including, comprising:

~~— a fractional portion of a semiconductor wafer having a plurality of integrated circuit chips thereon, such chips being separated by separating regions in the fractional portion of the wafer;~~

~~— a plurality of electrical components, each one being associated with, and adjacent to, a corresponding one of the chips; and~~

a fusible link electrically connecting a bus disposed in at least one of the plurality of integrated circuit chips and a corresponding one of the plurality of electrical components.

11. (Amended) The semiconductor recited in claim ~~10~~ 6 wherein each one of the electrical components is disposed in the separating region.

12. The semiconductor recited in claim 11 wherein the electrical components are voltage generators.

13. (Amended) The semiconductor recited in claim 12 wherein the voltage generators are interconnected by a ~~the~~ conductor elevated above the regions in the fractional portion of the wafer.

14. The semiconductor recited in claim 10 wherein the fusible link is disposed in disposed in at least one of the plurality of integrated circuit chips.

15. The semiconductor recited in claim 12 wherein at least one of the voltage generators is coupled to more than one bus in corresponding ones of the plurality of integrated circuit chips.